WHAT IS CLAIMED IS:

1. A technique for testability of a semiconductor integrated circuit, comprising:

the first step of conducting a fault simulation for the semiconductor integrated circuit based on a predetermined test pattern and discriminating a detectable fault and an undetectable fault from each other;

the second step of list undetectable faults as undetected faults;

the third step of determining the test conditions for testing the undetected faults;

the fourth step of determining a test pattern most likely to meet the test conditions of the third step from among predetermined test patterns of the fault simulation of the first step;

the fifth step of replacing registers associated with the undetected faults of the second step with scan registers and connecting the scan registers in a scan chain thereby to construct a modified circuit; and

the sixth step of conducting the fault simulation or the test by switching to the test condition determined in the third step at the timing corresponding to the undetected faults while using the determined test pattern in the fourth step for the modified circuit.

2. A technique for testability of a semiconductor integrated circuit according to claim 1,

wherein the fifth step includes the step of replacing the input-side registers associated with the undetected faults not by scan registers but by registers with set or reset function thereby to constitute a modified circuit.

3. A technique for testability of a semiconductor integrated circuit, wherein the registers connected to a combination logic circuit constituting an object of the

test in the semiconductor integrated circuit are classified into first registers that can be controlled and observed directly from a built-in processor, second registers that can be controlled and observed directly from a terminal of the semiconductor integrated circuit and third registers other than the first and second registers, the technique comprising:

the first step of replacing the third registers with scan registers and connecting the scan registers in a scan chain to thereby constitute a modified circuit;

the second step of setting and inputting the test data to the first and second registers from selected one of the processor and the integrated circuit terminal;

the third step of setting and inputting the test data to the third register with the shift operation through the scan chain;

the fourth step of performing the capture operation of the test data for the combination logic circuit;

the fifth step of outputting the test result data from the third register with the shift operation through the scan chain; and

the sixth step of outputting the test result data from the first and second registers.